<u>AMENDMENTS TO THE CLAIMS:</u>

The following listing of claims will replace all prior versions of claims in the application:

1. (Currently Amended) A method for resolving timing violations introduced by a logic built-in self test (LBIST) sub-circuit formed within an underlying integrated circuit, said method comprising:

analyzing a circuit path-list corresponding to said integrated circuit for timing violations and generating a ~~circuit~~ primary timing violations analysis output;

generating a first ~~LBIST/circuit path-list~~ netlist with LBIST based on said circuit path-list and an LBIST path-list corresponding to said LBIST sub-circuit;

analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST for timing violations and generating ~~an LBIST/circuit~~ a secondary timing violations analysis output;

comparing said ~~LBIST/circuit~~ secondary timing violations analysis output with said ~~circuit~~ primary timing violations analysis output;

generating an ~~LBIST/circuit~~ LBIST insertion constraint file based on said comparing ~~and predetermined protocols~~; and

generating a second ~~LBIST/circuit path-list~~ netlist with LBIST based on said circuit path-list, said LBIST path-list, and said constraints file wherein said timing violations introduced by said LBIST sub-circuit are resolved in said second ~~LBIST/circuit path-list~~ netlist with LBIST.

2. (Original) A method in accordance with claim 1,

wherein said circuit path-list includes a set of paths wherein each path in said set corresponds to a different route traversing a predetermined sequence of circuit components in said integrated circuit.

3. (Original) A method in accordance with claim 2,

wherein said LBIST path-list includes a set of paths wherein each path in said set corresponds to a different route traversing a predetermined sequence of circuit components in said LBIST sub-circuit.

4. (Currently Amended) A method in accordance with claim 3, wherein said generating a first ~~LBIST/circuit path-list~~ netlist with LBIST further comprises:

generating a first scanned circuit path-list; and

inserting said LBIST path-list into said first scanned circuit path-list to generate said first ~~LBIST/circuit path-list~~ netlist with LBIST.

5. (Currently Amended) A method in accordance with claim 4, wherein said constraint file comprises of a set of said circuits in said LBIST path-list and a set of paths in said circuit path-list and wherein said generating a second ~~LBIST/circuit path-list~~ netlist with LBIST further comprises:

generating a second scanned circuit path-list;

modifying paths in said second scanned circuit path-list based on said paths in said constraint file; and

inserting said LBIST path-list into said second scanned circuit path-list based on said constraint file to generate said second ~~LBIST/circuit path-list~~ netlist with LBIST wherein said circuits in said constraint file are excluded from said inserting into said scanned circuit path-list and said generated second ~~LBIST/circuit path-list~~ netlist with LBIST.

6. (Original) A method in accordance with claim 5, wherein said predetermined sequence of circuit components comprising:

a first circuit component wherein said first circuit component is the first traversed component in said path; and

a second circuit component wherein said second circuit component is the last traversed component in said path.

7. (Original) A method in accordance with claim 6, wherein said first traversed component is a scan-enabled electronic flip-flop.

8. (Original) A method in accordance with claim 6, wherein said first traversed component is a memory output port.

9. (Original) A method in accordance with claim 6, wherein said first traversed component is an external input port.

10. (Original) A method in accordance with claim 6, wherein said last traversed component is a scan-enabled electronic flip-flop.

11. (Original) A method in accordance with claim 6, wherein said last traversed component is a memory input port.

12. (Original) A method in accordance with claim 6, wherein said last traversed component is an external output port.

13. (Currently Amended) A method in accordance with claim 6,

wherein said analyzing said circuit path-list includes performing a functional mode timing violations analysis of said circuit path-list; and,

wherein said generating a ~~circuit~~ primary timing violation analysis output includes generating a circuit functional mode timing violations output path-list.

14. (Currently Amended) A method in accordance with claim 13, wherein said analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST further comprises:

analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST for functional mode timing violations and generating ~~an LBIST/circuit functional~~ a functional mode timing violations output path-list; and

analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST for an LBIST mode timing violations and generating an ~~LBIST/circuit~~ LBIST mode timing violations output path-list,

wherein said generated ~~LBIST/circuit~~ secondary timing violations analysis output includes said functional mode timing violations output path-list and said LBIST mode timing violations output path-list.

15. (Currently Amended) A method in accordance with claim 14, wherein said comparing further comprises:

comparing said ~~LBIST/circuit~~ functional mode timing violations output path-list with said ~~circuit~~ primary timing violations analysis output path-list and generating a first comparison output path-list; and

identifying in said first comparison output path-list a path with a circuit component causing timing violation, wherein said identifying is performed based on ~~said~~ predetermined identification protocols.

16. (Currently Amended) A method in accordance with claim 14, wherein said comparing further comprises:

comparing said ~~LBIST/circuit~~ LBIST mode timing violations output path-list with said ~~LBIST/circuit~~ functional mode timing violations output path-list and generating a second comparison output path-list; and

identifying in said second comparison output path-list a path with a timing violation.

17. (Currently Amended) A method in accordance with claim 15, wherein said comparing further comprises:

separating each path in said ~~LBIST/circuit~~ functional mode timing violations output path-list exclusive from said ~~circuit~~ primary timing violations analysis output path-list wherein said first comparison output includes said separated paths.

18. (Original) A method in accordance with claim 17, wherein said timing violation is a control point timing violation caused by a control point circuit.

19. (Original) A method in accordance with claim 17, wherein said timing violation is an observe point timing violation caused by an observe point circuit.

20. (Original) A method in accordance with claim 17, wherein said timing violation is an x-bounding timing violation caused by an x-bounding circuit.

21. (Original) A method in accordance with claim 18, said predetermined identification protocols comprising:

comparing each path in said separated paths in said first comparison output path-list with a predetermined control-point-insertion database to identify said control-point timing violation circuits in said path,

wherein said constraint file includes said identified control-point timing violation circuits in said path.

22. (Original) A method in accordance with claim 19, said predetermined identification protocols comprising:

comparing each path in said separated paths in said first comparison output path-list with a predetermined observe-point-insertion database to identify said observe-point timing violation circuits in said path,

wherein said constraint file includes said identified observe-point timing violation circuits in said path

23. (Original) A method in accordance with claim 20, said predetermined identification protocols comprising:

comparing each path in said separated paths in said first comparison output path-list with a predetermined x-bounding-insertion database to identify said x-bounding timing violation circuits in said path,

wherein said constraint file includes said identified x-bounding timing violation circuits in said path.

24. (Currently Amended) A method in accordance with claim 16, wherein said comparing further comprises:

separating each path in said ~~LBIST/circuit~~ LBIST mode timing violations output path-list exclusive from said ~~LBIST/circuit~~ functional mode timing violations output path-list wherein said constraints file includes said separated paths.

25. (Original) A method in accordance with claim 24, wherein said timing violation is a multi-cycle-path violation.

26. (Original) A method in accordance with claim 24, wherein said timing violation is a false-path violation.

27. (Original) A method in accordance with claim 23, wherein said modifying comprising:

suppressing a capture of said last traversed scan-enabled electronic flip-flop in each said path.

28. (Currently Amended) A method in accordance with claim 23, further comprising:

determining each path in said first ~~LBIST/circuit path-list~~ netlist with LBIST whose first traversed circuit component is a first circuit component in said predetermined sequence of circuit components in each said separated path; and

suppressing a capture of a last traversed scan-enabled electronic flip-flop in each of said determined paths.

29. (Original) A method in accordance with claim 24, further comprising:

suppressing a capture of a last traversed scan-enabled electronic flip-flop in said separated paths.

30. (Original) A method in accordance with claim 29, wherein said suppressed component is a receiving flip-flop.

31. (Currently Amended) A system for resolving timing violations introduced by a logic built-in self test (LBIST) sub-circuit formed within an underlying integrated circuit, said system comprising:

means for analyzing a circuit path-list corresponding to said integrated circuit for timing violations and generating a ~~circuit~~ primary timing violations analysis output;

means for generating a first ~~LBIST/circuit path-list~~ netlist with LBIST based on said circuit path-list and an LBIST path-list corresponding to said LBIST sub-circuit;

means for analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST for timing violations and generating ~~an LBIST/circuit~~ secondary timing violations analysis output;

means for comparing said ~~LBIST/circuit~~ secondary timing violations analysis output with said ~~circuit~~ primary timing violations analysis output;

means for generating an ~~LBIST/circuit~~ LBIST insertion constraint file based on said means for comparing ~~and predetermined protocols~~; and

means for generating a second ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> based on said

circuit path-list, said LBIST path-list, and said constraints file wherein said timing violations

introduced by said LBIST sub-circuit are resolved in said second ~~LBIST/circuit path-list~~ <u>netlist</u>

<u>with LBIST</u>.

32. (Original) A system in accordance with claim 31,

wherein said circuit path-list includes a set of paths wherein each path in said set

corresponds to a different route traversing a predetermined sequence of circuit components in

said integrated circuit.

33. (Original) A system in accordance with claim 32,

wherein said LBIST path-list includes a set of paths wherein each path in said set

corresponds to a different route traversing a predetermined sequence of circuit components in

said LBIST sub-circuit.

34. (Currently Amended) A system in accordance with claim 33, wherein said means for

generating a first ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> further comprises:

means for generating a first scanned circuit path-list; and

means for inserting said LBIST path-list into said first scanned circuit path-list to

generate said first ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u>.

35. (Currently Amended) A system in accordance with claim 34, wherein said constraint

file comprises of a set of said circuits in said LBIST path-list and a set of paths in said circuit

path-list and wherein said means for generating a second ~~LBIST/circuit path-list~~ <u>netlist with</u>

<u>LBIST</u> further comprises:

means for generating a second scanned circuit path-list;

means for modifying paths in said second scanned circuit path-list based on said paths in

said constraint file; and

means for inserting said LBIST path-list into said second scanned circuit path-list based

on said constraint file to generate said second ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> wherein

said circuits in said constraint file are excluded from said inserting into said scanned circuit path-

list and said generated second ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u>.

36. (Original) A system in accordance with claim 35, wherein said predetermined

sequence of circuit components comprising:

a first circuit component wherein said first circuit component is the first traversed

component in said path; and

a second circuit component wherein said second circuit component is the last traversed

component in said path.

37. (Original) A system in accordance with claim 36, wherein said first traversed

component is a scan-enabled electronic flip-flop.

38. (Original) A system in accordance with claim 36, wherein said first traversed

component is a memory output port.

39. (Original) A system in accordance with claim 36, wherein said first traversed component is an external input port.

40. (Original) A system in accordance with claim 36, wherein said last traversed component is a scan-enabled electronic flip-flop.

41. (Original) A system in accordance with claim 36, wherein said last traversed component is a memory input port.

42. (Original) A system in accordance with claim 36, wherein said last traversed component is an external output port.

43. (Currently Amended) A system in accordance with claim 36,

wherein said means for analyzing said circuit path-list includes means for performing a functional mode timing violations analysis of said circuit path-list; and,

wherein said means for generating a ~~circuit~~ primary timing violation analysis output includes means for generating a circuit functional mode timing violations output path-list.

44. (Currently Amended) A system in accordance with claim 43, wherein said means for analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST further comprises:

means for analyzing said first ~~LBIST/circuit path-list~~ netlist with LBIST for functional mode timing violations and generating ~~an LBIST/circuit functional~~ a functional mode timing violations output path-list; and

means for analyzing said first ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> for an LBIST

mode timing violations and generating an ~~LBIST/circuit~~ LBIST mode timing violations output

path-list,

wherein said generated ~~LBIST/circuit~~ <u>secondary</u> timing violations analysis output

includes said functional mode timing violations output path-list and said LBIST mode timing

violations output path-list.

45. (Currently Amended) A system in accordance with claim 44, wherein said means for

comparing further comprises:

means for comparing said ~~LBIST/circuit~~ functional mode timing violations output path-

list with said ~~circuit~~ <u>primary</u> timing violations analysis output path-list and generating a first

comparison output path-list; and

means for identifying in said first comparison output path-list a path with a circuit

component causing timing violation, wherein said identifying is performed based on ~~said~~

predetermined identification protocols.

46. (Currently Amended) A system in accordance with claim 44, wherein said means for

comparing further comprises:

means for comparing said ~~LBIST/circuit~~ LBIST mode timing violations output path-list

with said ~~LBIST/circuit~~ functional mode timing violations output path-list and generating a

second comparison output path-list; and

means for identifying in said second comparison output path-list a path with a timing

violation.

47. (Currently Amended) A system in accordance with claim 45, wherein said means for comparing further comprises:

means for separating each path in said ~~LBIST/circuit~~ functional mode timing violations output path-list exclusive from said ~~circuit~~ primary timing violations analysis output path-list wherein said first comparison output includes said separated paths.

48. (Original) A system in accordance with claim 47, wherein said timing violation is a control point timing violation caused by a control point circuit.

49. (Original) A system in accordance with claim 47, wherein said timing violation is an observe point timing violation caused by an observe point circuit.

50. (Original) A system in accordance with claim 47, wherein said timing violation is an x-bounding timing violation caused by an x-bounding circuit.

51. (Original) A system in accordance with claim 48, said predetermined identification protocols comprising:

a protocol for comparing each path in said separated paths in said first comparison output path-list with a predetermined control-point-insertion database to identify said control-point timing violation circuits in said path,

wherein said constraint file includes said identified control-point timing violation circuits in said path.

52. (Original) A system in accordance with claim 49, said predetermined identification protocols comprising:

a protocol for comparing each path in said separated paths in said first comparison output path-list with a predetermined observe-point-insertion database to identify said observe-point timing violation circuits in said path,

wherein said constraint file includes said identified observe-point timing violation circuits in said path.

53. (Original) A system in accordance with claim 50, said predetermined identification protocols comprising:

a protocol for comparing each path in said separated paths in said first comparison output path-list with a predetermined x-bounding-insertion database to identify said x-bounding timing violation circuits in said path,

wherein said constraint file includes said identified x-bounding timing violation circuits in said path.

54. (Currently Amended) A system in accordance with claim 46, wherein said means for comparing further comprises:

means for separating each path in said ~~LBIST/circuit~~ LBIST mode timing violations output path-list exclusive from said ~~LBIST/circuit~~ functional mode timing violations output path-list wherein said constraints file includes said separated paths.

55. (Original) A system in accordance with claim 54, wherein said timing violation is a multi-cycle-path violation.

56. (Original) A system in accordance with claim 54, wherein said timing violation is a false-path violation.

57. (Original) A system in accordance with claim 53, wherein said means for modifying comprising:

means for suppressing a capture of said last traversed scan-enabled electronic flip-flop in each said path.

58. (Currently Amended) A system in accordance with claim 53, further comprising:

means for determining each path in said first ~~LBIST/circuit path list~~ netlist with LBIST whose first traversed circuit component is a first circuit component in said predetermined sequence of circuit components in each said separated path; and

means for suppressing a capture of a last traversed scan-enabled electronic flip-flop in each of said determined paths.

59. (Original) A system in accordance with claim 54, further comprising:

means for suppressing a capture of a last traversed scan-enabled electronic flip-flop in said separated paths.

60. (Original) A system in accordance with claim 59, wherein said suppressed component is a receiving flip-flop.

61. (Currently Amended) A system for resolving timing violations introduced by a logic built-in self test (LBIST) sub-circuit formed within an underlying integrated circuit, said system comprising:

a first analyzer subsystem adapted to receive and analyze a circuit path-list corresponding to said integrated circuit for timing violations and generate a ~~circuit~~ primary timing violations analysis output;

a first path-list generator subsystem in operative electrical communication with said first analyzer subsystem and adapted to generate a first ~~LBIST/circuit path-list~~ netlist with LBIST based on said circuit path-list and an LBIST path-list corresponding to said LBIST sub-circuit;

an second analyzer subsystem in operative electrical communication with said first path-list generator subsystem and adapted to receive and analyze said first ~~LBIST/circuit path-list~~ netlist with LBIST for timing violations and generating ~~an LBIST/circuit~~ secondary timing violations analysis output;

a comparator subsystem in operative electrical communication with said second analyzer subsystem and said first analyzer subsystem, and adapted to receive and to compare said ~~LBIST/circuit~~ secondary timing violations analysis output with said ~~circuit~~ primary timing violations analysis output, and to output a comparison result;

a second path-list generator subsystem in operative electrical communication with said comparator subsystem and adapted to generate an ~~LBIST/circuit~~ LBIST insertion constraint file based on said comparison result ~~output and predetermined protocols~~; and

a third path-list generator subsystem in operative electrical communication with said second path-list generator subsystem and adapted to generate a second ~~LBIST/circuit path-list~~ netlist with LBIST based on said circuit path-list, said LBIST path-list, and said constraints file

wherein said timing violations introduced by said LBIST·sub-circuit are resolved in said second ~~LBIST/circuit path-list~~ netlist with LBIST.

62. (Original) A system in accordance with claim 61,

wherein said circuit path-list includes a set of paths wherein each path in said set corresponds to a different route traversing a predetermined sequence of circuit components in said integrated circuit.

63. (Original) A system in accordance with claim 61,

wherein said LBIST circuit path-list includes a set of paths wherein each path in said set corresponds to a different route traversing a predetermined sequence of circuit components in said LBIST sub-circuit.

64. (Currently Amended) A system in accordance with claim 63, wherein said first path-list generator subsystem further comprises:

a fourth generator subsystem adapted to generate a first scanned circuit path-list; and

a first insertion subsystem adapted to insert said LBIST path-list into said first scanned circuit path-list to generate said first ~~LBIST/circuit path-list~~ netlist with LBIST.

65. (Currently Amended) A system in accordance with claim 64, wherein said constraint file comprises of a set of said circuits in said LBIST path-list and a set of paths in said circuit path-list and wherein said third path-list generator subsystem further comprises:

a fifth generator subsystem adapted to generate a second scanned circuit path-list;

a modifier subsystem adapted to modify paths in said second scanned circuit path-list based on said paths in said constraint file; and

a second insertion subsystem adapted to insert said LBIST path-list into said second scanned circuit path-list based on said constraint file to generate said second ~~LBIST/circuit path-list~~ netlist with LBIST wherein said circuits in said constraint file are excluded from said insertion into said scanned circuit path-list and said generated second ~~LBIST/circuit path-list~~ netlist with LBIST.

66. (Original) A system in accordance with claim 65, wherein said predetermined sequence of circuit components comprising:

a first circuit component wherein said first circuit component is the first traversed component in said path; and

a second circuit component wherein said second circuit component is the last traversed component in said path.

67. (Original) A system in accordance with claim 66, wherein said first traversed component is a scan-enabled electronic flip-flop.

68. (Original) A system in accordance with claim 66, wherein said first traversed component is a memory output port.

69. (Original) A system in accordance with claim 66, wherein said first traversed component is an external input port.

70. (Original) A system in accordance with claim 66, wherein said last traversed component is a scan-enabled electronic flip-flop.

71. (Original) A system in accordance with claim 66, wherein said last traversed component is a memory input port.

72. (Original) A system in accordance with claim 66, wherein said last traversed component is an external output port.

73. (Currently Amended) A system in accordance with claim 66,

wherein said first analyzer subsystem is adapted to perform a functional mode timing violations analysis of said circuit path-list; and

wherein said generation of a ~~circuit~~ primary timing violation analysis output includes generation of a circuit functional mode timing violations output path-list.

74. (Currently Amended) A system in accordance with claim 73, wherein said second analyzer subsystem further comprises:

a third analyzer subsystem adapted to analyze said first ~~LBIST/circuit path-list~~ netlist with LBIST for functional mode timing violations and to generate ~~an LBIST/circuit functional~~ a functional mode timing violations output path-list; and

a fourth analyzer subsystem adapted to analyze said first ~~LBIST/circuit path-list~~ netlist with LBIST for an LBIST mode timing violations and to generate an ~~LBIST/circuit~~ LBIST mode timing violations output path-list,

wherein said generated ~~LBIST/circuit~~ secondary timing violations analysis output includes said functional mode timing violations output path-list and said LBIST mode timing violations output path-list.

75. (Currently Amended) A system in accordance with claim 74, wherein said comparator subsystem compares said ~~LBIST/circuit~~ functional mode timing violations output path-list with said ~~circuit~~ primary timing violations analysis output path-list and generates a first comparison output path-list; and

wherein said comparator subsystem identifies in said first comparison output path-list a path with a circuit component causing timing violation, wherein said identification is performed based on ~~said~~ predetermined identification protocols.

76. (Currently Amended) A system in accordance with claim 74, wherein said comparator subsystem compares said ~~LBIST/circuit~~ LBIST mode timing violations output path-list with said ~~LBIST/circuit~~ functional mode timing violations output path-list, generates a second comparison output path-list; and identifies in said second comparison output path-list a path with a timing violation.

77. (Currently Amended) A system in accordance with claim 75, wherein said comparator subsystem further comprises:

a separator subsystem adapted to separate each path in said ~~LBIST/circuit~~ functional mode timing violations output path-list exclusive from said ~~circuit~~ primary timing violations analysis output path-list wherein said first comparison output includes said separated paths.

78. (Original) A system in accordance with claim 77, wherein said timing violation is a control point timing violation caused by a control point circuit.

79. (Original) A system in accordance with claim 77, wherein said timing violation is an observe point timing violation caused by an observe point circuit.

80. (Original) A system in accordance with claim 77, wherein said timing violation is an x-bounding timing violation caused by an x-bounding circuit.

81. (Original) A system in accordance with claim 78, said predetermined identification protocols comprising:

a protocol to compare each path in said separated paths in said first comparison output path-list with a predetermined control-point-insertion database to identify said control-point timing violation circuits in said path,

wherein said constraint file includes said identified control-point timing violation circuits in said path.

82. (Original) A system in accordance with claim 79, said predetermined identification protocols comprising:

a protocol to compare each path in said separated paths in said first comparison output path-list with a predetermined observe-point-insertion database to identify said observe-point timing violation circuits in said path,

wherein said constraint file includes said identified observe-point timing violation circuits in said path.

83. (Original) A system in accordance with claim 80, said predetermined identification protocols comprising:

a protocol to compare each path in said separated paths in said first comparison output path-list with a predetermined x-bounding-insertion database to identify said x-bounding timing violation circuits in said path,

wherein said constraint file includes said identified x-bounding timing violation circuits in said path.

84. (Currently Amended) A system in accordance with claim 76, wherein said comparator subsystem further comprises:

a separator subsystem adapted to separate each path in said ~~LBIST/circuit~~ LBIST mode timing violations output path-list exclusive from said ~~LBIST/circuit~~ functional mode timing violations output path-list wherein said constraints file includes said separated paths.

85. (Original) A system in accordance with claim 84, wherein said timing violation is a multi-cycle-path violation.

86. (Original) A system in accordance with claim 84, wherein said timing violation is a false-path violation.

87. (Original) A system in accordance with claim 83, wherein said modifier subsystem comprising:

a suppression subsystem adapted to suppress a capture of said last traversed scan-enabled electronic flip-flop in each said path.

88. (Currently Amended) A system in accordance with claim 83, further comprising:

a determination subsystem adapted to determine each path in said first ~~LBIST/circuit path-list~~ netlist with LBIST whose first traversed circuit component is a first circuit component in said predetermined sequence of circuit components in each said separated path; and

a suppression subsystem adapted to suppress a capture of a last traversed scan-enabled electronic flip-flop in each of said determined paths.

89. (Original) A system in accordance with claim 84, further comprising:

a suppression subsystem adapted to suppress a capture of a last traversed scan-enabled electronic flip-flop in said separated paths.

90. (Original) A system in accordance with claim 89, wherein said suppressed component is a receiving flip-flop.

91. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for resolving timing violations introduced by a logic built-in self test (LBIST) sub-circuit formed within an underlying integrated circuit, said method comprising:

analyzing a circuit path-list corresponding to said integrated circuit for timing violations and generating a ~~circuit~~ primary timing violations analysis output;

generating a first ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> based on said circuit path-list

and an LBIST path-list corresponding to said LBIST sub-circuit;

analyzing said first ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> for timing violations and

generating ~~an LBIST/circuit~~ <u>secondary</u> timing violations analysis output;

comparing said ~~LBIST/circuit~~ <u>secondary</u> timing violations analysis output with said

~~circuit~~ <u>primary</u> timing violations analysis output;

generating an ~~LBIST/circuit~~ <u>LBIST insertion</u> constraint file based on said comparing ~~and~~

~~predetermined protocols~~; and

generating a second ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u> based on said circuit path-

list, said LBIST path-list, and said constraints file wherein said timing violations introduced by

said LBIST sub-circuit are resolved in said second ~~LBIST/circuit path-list~~ <u>netlist with LBIST</u>.